
Elements Of Logic Via Numbers And Sets

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800-967-5352 fax: 978-264-9403 **7. latches and flip-flops - ucr** - chapter 7 - latches and flip-flops page 3 of
18 a 0. when both inputs are de-asserted, the sr latch maintains its previous state. previous to t1, q has the
value 1, so at t1, q remains at a 1. similarly, previous to t3, q has the value 0, so at t3, q remains at a 0. if both
s' and r' are asserted, then both q and q' are equal to 1 as shown at time t4. if one of the input signals is **basic**
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